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DETAILED DESCRIPTION

[Detailed Description of the Invention]
[0001]
[Industrial Application] Especially this invention is applied to the semiconductor integrated circuit equipment which has a multilayer interconnection about semiconductor integrated circuit equipment and its manufacture method, and relates to effective technology.
[0002]
[Description of the Prior Art] The gate array method is mainly adopted as Boolean part of the memory LSI with logic (Large Scale Integrated Circuit). A gate array prepares the master slice beforehand formed to the diffusion process, by connection using wiring at a wiring process, is LSI which realizes a desired circuit and can develop the logical circuit of high accumulation for a short period of time.
[0003] By the way, in the memory LSI with logic which adopted the gate array method, since element density can be raised indeed and a performance will improve if a wiring number of layers increases, memory LSI with logic which development of the multilayering technology of the wiring which increased the number of layers is performed, for example, already has five-layer wiring is put in practical use.
[0004] the memory LSI with logic memory have this five layer wiring in conventional technology -- connection -- a hole -- the connection from the viewpoint of the covering nature reservation since formation can but form with former spatter technology -- a hole -- the need of carry out formation with a taper -- it be -- the connection -- a hole -- a wiring pitch set to 4.0 micrometers and , for example , have serve as a limitation the required shell a shell secure a field , and when raise a degree of integration
[0005] In addition, the wiring formed only with aluminum has the problem that electromigration resistance is weak and electric resistance increases by detailed-ization. Then, in order to improve electromigration resistance and to lower electric resistance. into aluminum, the film which made the copper (Cu) of 3% of concentration contain is deposited on up to a semiconductor substrate by the sputtering method, this is processed, and wiring is formed.
[0006] In addition, LSI using the multilayer interconnection is indicated by issue, the Nagata ****, and P129 on Baifukan Co., Ltd. issue "ultra high-speed bipolar device" November 15, Showa 60, for example.
[0007]
[Problem(s) to be Solved by the Invention] this invention person found out that the following troubles arose in the multilayer interconnection adopted as the aforementioned memory LSI with logic.
[0008] In order to carry a semiconductor device in high accumulation on a semiconductor chip, it is indispensable that reduction-ization of a wiring pitch sets the wiring pitch of signal wiring to 2.0 micrometers or less for obtaining the degree of integration more than the conventional double precision indispensably.
[0009] moreover, the connection prepared in a layer insulation film in order for the wiring pitch located up and down on both sides of a layer insulation film to connect the wiring which is 2.0 micrometers -- it is necessary to set the aperture of a hole to 1.0 micrometers or less However, the thickness of a layer insulation film cannot reduce thickness of a layer insulation film, although detailed-ization of a semiconductor device progresses, since it is the important parameter which governs the velocity of propagation of wiring.
[0010] therefore, the connection prepared in a layer insulation film -- since the aperture of a hole cannot make thickness of a layer insulation film thin even if it turns minutely, as high integration of LSI progresses -- connection -- the aspect ratio (connection the depth/aperture of a hole) of a hole -- high -- becoming -- connection of a high aspect ratio -- it is difficult to embed aluminum certainly by the sputtering method to a hole, and to form wiring of low resistance
[0011] Moreover, since the aluminum wiring containing Cu of 3% of concentration has the high reflection factor, if a monolayer resist is used at a phot lithography processes, the standing wave effect by interference of the incident light of exposure light and the reflected light will show up notably. Furthermore, if a monolayer resist is used in case the aforementioned aluminum wiring is processed by the dry etching method, since the selection ratio at the time of etching of the aforementioned aluminum wiring and a monolayer resist cannot be taken, poor processing of ARUNIMIUMU wiring will arise.
[0012] From these things, a monolayer resist cannot be used at the process which processes aluminum wiring, but adoption of a multilayer resist is indispensable. However, if each class of a multilayer interconnection is altogether processed using a multilayer resist, the number of processes not only increases remarkably, but the yield of a product will fall.
[0013] The purpose of this inventionis to offer the technology in which multilayering of the high density assembly of wiring and

wiring is simultaneously realizable.
[0014] Other purposes of this invention are in the semiconductor integrated circuit equipment which has a multilayer interconnection to offer the technology in which improvement in the manufacture yield, improvement in the speed of a working speed, and improvement in the throughput of a wiring process are simultaneously realizable.
[0015] The other purposes and the new feature will become clear from description and the accompanying drawing of this specification at the aforementioned row of this invention.
[0016]
[Means for Solving the Problem] It will be as follows if the outline of a typical thing is briefly explained among invention indicated in this application. Namely, the semiconductor integrated circuit equipment of (1) this invention The even-numbered wiring which has the multilayer interconnection constituted by wiring of three or more layers, and is formed in the upper layer rather than the 2nd-layer wiring and the 2nd-layer aforementioned wiring The odd-numbered wiring which extends in the direction of X, or the direction of Y, and is formed in the upper layer rather than the 3rd-layer wiring and the 3rd-layer aforementioned wiring the 2nd-layer aforementioned wiring is intersected -- as -- the direction of Y, or the direction of X -- extending -- **** -- further -- wiring PI@TCHI of the even-numbered [aforementioned] wiring -- the wiring pitch of the 2nd-layer aforementioned wiring -- the same -- moreover, the wiring pitch of the odd-numbered [aforementioned] wiring is the same as the wiring pitch of the 3rd-layer aforementioned wiring
[0017] (2) Moreover, the semiconductor integrated circuit equipment of this invention In the semiconductor integrated circuit equipment of the above (1), the m-th-layer wiring which is the even-numbered [aforementioned] wiring formed in the upper layer rather than the 2nd-layer aforementioned wiring Only one half of the distance of the wiring pitch of the ** (m-2) layer wiring which is the even-numbered [aforementioned] wiring arranged under the m-th-layer aforementioned wiring, and the 2nd-layer aforementioned wiring shifts, and is arranged. Moreover, only one half located under the n-th-layer aforementioned wiring of the distance of the wiring pitch of the ** (n-2) layer wiring which is the odd-numbered [aforementioned] wiring, and the 3rd-layer aforementioned wiring shifts, and the n-th-layer wiring which is the odd-numbered [aforementioned] wiring formed in the upper layer rather than the 3rd-layer aforementioned wiring is arranged.
[0018] (3) Moreover, the manufacture method of the semiconductor integrated circuit equipment of this invention In the above (1) or the semiconductor integrated circuit equipment of (2) the 1st-layer wiring Tungsten wiring, The wiring formed in the upper layer rather than the 2nd-layer aforementioned wiring and the 2nd-layer aforementioned wiring is formed with a tungsten / aluminum / tungsten laminating wiring. The lower layer tungsten film which constitutes the aforementioned tungsten wiring, and the aforementioned tungsten / aforementioned aluminum / tungsten laminating wiring It forms by depositing the tungsten film formed by the tungsten film and the CVD (Chemical Vapor Deposition) method which are formed by the sputtering method one by one on a semiconductor substrate.
[0019] (4) Moreover, in the manufacture method of the semiconductor integrated circuit equipment the above (3), the manufacture method of the semiconductor integrated circuit equipment of this invention is an aluminum film containing Cu of 3% or less of concentration, and constitutes the interlayer of the aforementioned tungsten / aluminum / tungsten laminating wiring.
[0020]
[Function] according to above-mentioned means (1) - (3) -- connection -- a hole -- since formation can be embedded by the CVD film also as perpendicular processing -- connection -- a hole -- the wiring formed in the upper layer rather than the 2nd-layer wiring and the 2nd-layer wiring since-izing of the formation field can be carried out [****] becomes possible [arranging in a wiring pitch 2.0 micrometers or less]
[0021] moreover, the connection prepared in order to connect the n-th-layer wiring (n is three or more integers) and ** (n+1) layer wiring -- the connection prepared in order that a hole may connect the n-th-layer wiring and ** (n-1) layer wiring -- since it can arrange to a hole in the part which shifted only one half of the distance of a wiring pitch -- connection -- the flexibility of the layout of a hole can be increased
[0022] depositing in CVD the lower layer tungsten film which constitutes tungsten wiring, and a tungsten / aluminum / tungsten laminating wiring according to the above-mentioned means (3) and (4) -- an aspect ratio -- connection of 2.0 -- wiring can be embedded with sufficient covering nature also at a hole Furthermore, since the adhesive property of the tungsten film formed by CVD by depositing a tungsten film by the sputtering method improves before depositing a tungsten film in CVD, peeling and defective continuity of wiring can be prevented.
[0023] Moreover, since the aluminum film of low resistance is prepared for the interlayer of a tungsten / aluminum / tungsten laminating wiring, resistance of wiring can be reduced.
[0024] Moreover, since concentration of Cu which the aluminum film of the interlayer of a tungsten / aluminum / tungsten laminating wiring contains is made into 3% or less, even if it uses a monolayer resist for a mask and processes laminating wiring by the dry etching method, the dry etching resistance of a good monolayer resist is acquired. Furthermore, since the tungsten film is prepared in the upper layer, even if it uses a monolayer resist, the standing wave effect stops easily being able to reduce reflection of the exposure light from the wiring in a phot lithography processes, and being able to appear.
[0025]
[Example] Hereafter, the example of this invention is explained in detail based on a drawing.
[0026] The memory LSI with logic which is one example of this invention is explained using drawing 1 - drawing 5 . In addition, what has the same function in the complete diagram for explaining an example attaches the same sign, and explanation of the repeat is omitted.

[0027] Drawing 1 is drawing showing the chip layout of the memory LSI 1 with logic. The flat-surface configuration is formed on the square semiconductor substrate 2, and the memory LSI 1 with logic consists of Boolean part 3, the memory cell section 4, a memory cell control section 5, and the I/O circuit section 6. Boolean part 3 consists of gate arrays, it is the structure where two or more primitive cells 7 have been arranged, and it forms a primitive cell train and multi-line arrangement is carried out that there is no crevice in the direction of X.
[0028] Semiconductor devices, such as a transistor and resistance, are formed in the primitive cell 7, and this transistor is a bipolar transistor of GST (Gate Self-Aligned Technology) structure. In addition, the bipolar transistor of GST structure can reduce the area of the active region in which a semiconductor device is formed, and since the parasitic capacitance produced between active regions is reduced, it can attain improvement in the speed of a working speed.
[0029] The connection method of the signal wiring in Boolean part 3 constituted from a gate array by drawing 2 is shown. The memory LSI 1 with logic of this example has adopted six-layer wiring, in Boolean part 3, only the 1st-layer wiring 8 performs connection between primitive cells 7, and the 6th-layer wiring 13 is used for the 5th-layer wiring 12 (M5) and power supply wiring from the 2nd-layer wiring 9 (M2) at signal wiring. Wiring width of face of signal wiring is set to 1.0 micrometers, and the space is set to 1.0 micrometers, therefore the wiring pitch (P1) of signal wiring is set to 2.0 micrometers.
[0030] As shown in drawing 2 , the 2nd-layer wiring 9 extends in the direction of Y in a 2.0-micrometer wiring pitch, on the other hand the 3rd-layer wiring 10 is constituted so that it may extend in the direction of X in a 2.0-micrometer wiring pitch. Furthermore, the 4th-layer wiring 11 shifted the distance of the half (P1 / 2= 1.0 micrometers) of a wiring pitch to the 2nd-layer wiring 9, and has extended in the direction of Y in the 2.0-micrometer wiring pitch like the 2nd-layer wiring 9.
[0031] The 5th-layer wiring 12 also shifts the distance of the half (P1 / 2= 1.0 micrometers) of a wiring pitch to the 3rd-layer wiring 10, and it is constituted so that it may extend in the direction of X like the 3rd-layer wiring 10.
[0032] However, in signal wiring, when requiring low wiring of resistance, as shown in the 5th-layer wiring 12 of drawing 2 . latus wiring (for example, 3.0 micrometers) of width of face is used. In addition, the thickness of signal wiring is about 0.9 micrometers.
[0033] The space of the 6th-layer wiring 13 used as power supply wiring is 8.0 micrometers, and thickness is about 2.0 micrometers.
[0034] the connection prepared in a layer insulation film in order to connect the wiring located in the upper and lower sides from the 1st-layer wiring 8 to the 5th-layer wiring 12 -- the connection to which all of the aperture of holes 14, 15, 16, and 17 connect the 6th-layer wiring 13 of 0.6 micrometers, and the best 5th layer layer they are [layer] wiring 12 and power supply wiring -- the size of a hole 18 is 1.5x3.0 micrometers moreover, connection -- the space of 1.2 micrometers and wiring of the width of face of wiring of the place where holes 14, 15, 16, and 17 are arranged is 0.8 micrometers
[0035] connection -- the connection prepared in the upper and lower sides of a certain signal wiring as arrangement of a hole -- a hole can be arranged in the part which the wiring pitch left 1/2
[0036] for example, the connection prepared between the 2nd-layer wiring 9 and the 3rd-layer wiring 10 as shown in drawing 3 -- the connection prepared between the 3rd-layer wiring 10 and the 4th-layer wiring 11 to a hole 15 -- a hole 16 can be formed in the part which is 1/2 of a wiring pitch and which was detached 1.0 micrometers
[0037] Next, the important section cross-section structure and its manufacture method of Boolean part 3 of this example are explained using drawing 4 . [of the memory LSI 1 with logic]
[0038] As shown in drawing 4 , the memory LSI 1 with logic of this example is constituted considering p type semiconductor substrate 101a which consists of single crystal silicon as a subject. On the principal plane of this semiconductor substrate 101a, the laminating of the n type epitaxial layer 103 is carried out, and the active region (element formation field) is further prepared in the principal plane of semiconductor substrate 101a. The rear face of semiconductor substrate 101a consists of oxidization silicon film 101c and support substrate 101b.
[0039] It embeds at an active region between the aforementioned semiconductor substrate 101a and n type epitaxial layer 103, and the n-type-semiconductor field 102 of a mold is formed. The aforementioned active region is electrically separated by the isolation field with other surrounding active regions. The isolation field mainly consists of element separation insulator layers (for example, oxidization silicon film) 104 and 105.
[0040] The bipolar transistor is formed in the aforementioned active region. This bipolar transistor consists of vertical structures which arranged each of n type collector field, p type base region, and n type emitter region one by one.
[0041] n type collector field consists of an n type epitaxial layer 103, an embedding type n-type-semiconductor field 102, and a n-type-semiconductor field 106 for collector potential raising. p type base region consists of p type semiconductor fields 108 which are the p type semiconductor field 107 and the intrinsic base region which are a graft-base field. n type emitter region consists of n-type-semiconductor fields 109.
[0042] Tungsten wiring (it abbreviates to W wiring below) 115a is connected to the aforementioned n-type-semiconductor field 106 for collector potential raising through collector opening 104a.
[0043] The end of the electrode 110 for base drawers is connected to the p type semiconductor field 107 which is p type base region through base opening 104b. the connection formed in the other end of the electrode 110 for base drawers at insulator layers 112a and 112b -- W wiring 115b is formed through the hole 113
[0044] The electrode 111 for emitter drawers is connected to the n-type-semiconductor field 109 which is n type emitter region through emitter opening 104c. the connection to which the electrode 111 for emitter drawers was formed in insulator layer 112a -- it connects with W wiring 115c electrically through the hole 114 In addition, the emitter drawer electrode 111 is formed with

the polycrystal silicon with which n type impurity (As or P) was introduced.
[0045] The aforementioned W wiring 115a, 115b, and 115c is formed by the manufacturing process of the 1st-layer wiring 8. After these W wiring 115a, 115b, and 115c deposits 0.2 micrometers of tungsten films on semiconductor substrate 101a by the sputtering method, succeedingly, within the same equipment, by CVD, it deposits 0.2 micrometers of tungsten films, and forms them.
[0046] the connection which has an aspect ratio with the expensive tungsten film which the tungsten film deposited by the sputtering method is bearing the duty as a glue line between the tungsten film deposited in CVD, and a lower layer insulator layer, and was deposited in CVD -- it has good covering nature to the hole
[0047] The W wiring 115a, 115b, and 115c is covered by the 1st layer insulation film 116, 117, and 118. The 1st layer insulation film 116 is an oxidization silicon film formed of CVD, had good covering nature and is covered with the W wiring 115a-115c.
 [0048] The 1st layer insulation film 117 embeds the crevice produced on the 1st layer insulation film 116, and it is prepared in order to carry out flattening of the front face of the 1st layer insulation film 116. That is, an oxidization silicon film is deposited by the applying (Spin On Glass;SOG) method on the 1st layer insulation film 116, and the 1st layer insulation film 117 is embedded by carrying out etchback of this in the crevice produced on the 2nd layer insulation film 116.
[0049] The 1st layer insulation film 118 is formed in order to secure the pressure-proofing between layers of wiring, and it is an oxidization silicon film formed of CVD.
[0050] The thickness of the 1st layer insulation film 117 which deposited the thickness of the 1st layer insulation film 116 by about 0.4 micrometers and the applying method is [the thickness of about 0.55 micrometers and the 1st layer insulation film 118 of the thickness of about 0.4 micrometers and etchback] about 0.9 micrometers.
[0051] On the 1st layer insulation film 116 and 117 and 118, the tungsten / aluminum / tungsten laminating wiring 120 (it abbreviates to W/aluminum/W laminating wiring below) formed by the manufacturing process of the 2nd-layer wiring 9 are formed. the connection to which the W/aluminum/W laminating wiring 120 was formed in the 1st layer insulation film 116 and 118 -- it has connected with the W wiring 115a-115c which is the 1st-layer wiring 8 through a hole 119 this connection -- a hole 119 is mostly processed into a perpendicular -- having -- **** -- connection -- the aperture of a hole 119 is 0.6 micrometers and an aspect ratio is 2.0
[0052] Just before forming the W/aluminum/W laminating wiring 120, sputter-etching processing is performed into inert gas atmosphere. This sputter-etching processing is performed in order to remove the insulating material (for example, tungstic oxide) formed in the front face of the W wiring 115a-115c which is the 1st-layer wiring 8.
[0053] in addition, sputter-etching processing -- facing -- connection -- in order to reduce that insulating material adheres to the front face of the W wiring 115a-115c again by striking the 1st layer insulation film 116 and 118 which accomplishes the side attachment wall of a hole 119 by the charged particle -- connection -- as for the configuration of a hole 119, forming perpendicularly is desirable
[0054] the lower layer tungsten film which constitutes the W/aluminum/W laminating wiring 120 forms membranes by consecutive processing of the sputtering method and CVD -- having -- the 1st layer insulation film 116 and 118 of a ground -- receiving -- connection of an aspect ratio high [having a good adhesive property] -- it has good covering nature to the hole 119
[0055] Moreover, an interlayer's aluminum film is an aluminium alloy film containing both an aluminum monolayer or silicon (Si), Cu, or Si and Cu, and it is used in order to lower resistance of wiring. The concentration of Cu in an aluminium alloy film is 3.0% or less, and Cu is effective in reducing the electromigration of wiring. The upper tungsten film has the effect which suppresses reflection of the exposure light from the front face of the wiring in a photolithography process.
[0056] The lower layer tungsten film which constitutes the W/aluminum/W laminating wiring 120 consists of a tungsten film with a thickness of 0.05 micrometers deposited by the sputtering method, and a 0.2-micrometer tungsten film deposited in CVD, and the thickness of 0.6 micrometers and the upper tungsten film of the thickness of an interlayer's aluminum film is 0.05 micrometers.
[0057] In addition, the front face of the 1st layer insulation film 116, 117, and 118 located under the W/aluminum/W laminating wiring 120 is flat, and since the tungsten film which is a low reflective film is adopted as the upper layer, in a phot lithography processes which process the W/aluminum/W laminating wiring 120, the standing wave effect is suppressed and it becomes possible to use a monolayer resist.
[0058] The W/aluminum/W laminating wiring 120 is covered by the 2nd layer insulation film 121, 122, and 123. The 2nd layer insulation film 121 is the 1st layer insulation film 116 formed on W wiring 115a which is the 1st-layer wiring 8 - 115c, and an oxidization silicon film similarly formed of CVD, had good covering nature and is covered with the W/aluminum/W laminating wiring 120.
[0059] The 2nd layer insulation film 122 embeds the crevice produced on the 2nd layer insulation film 121, and it is prepared in order to carry out flattening of the front face of the 2nd layer insulation film 121. That is, an oxidization silicon film is deposited on the 2nd layer insulation film 121 by the applying method, and the 2nd layer insulation film 122 is embedded by carrying out etchback of this in the crevice produced on the 2nd layer insulation film 121.
[0060] The 2nd layer insulation film 123 is formed in order to secure the pressure-proofing between layers of wiring, and it is an oxidization silicon film formed of CVD.
[0061] The thickness of the 2nd layer insulation film 122 which deposited the thickness of the 2nd layer insulation film 121 by about 0.6 micrometers and the applying method is [the thickness of about 0.6 micrometers and the 2nd layer insulation film 123 of the thickness of about 0.55 micrometers and etchback] about 0.9 micrometers.

[0062] On the 2nd layer insulation film 121 and 122 and 123, the W/aluminum/W laminating wiring 124 formed by the manufacturing process of the 3rd-layer wiring 10 is formed. the connection to which the W/aluminum/W laminating wiring 124 was formed in the 2nd layer insulation film 121 and 123 -- it has connected with the W/aluminum/W laminating wiring 120 which is the 2nd-layer wiring 9 through a hole 125 this connection -- the hole 125 is mostly processed into the perpendicular
[0063] The W/aluminum/W laminating wiring 124 is formed by the same method as the W/aluminum/W laminating wiring 120 which is the 2nd-layer wiring 9. Moreover, just before forming the W/aluminum/W laminating wiring 124, sputter-etching processing is performed into inert gas atmosphere like the time of formation of the W/aluminum/W laminating wiring 120 which is the 2nd-layer wiring 9.
[0064] by the way, connection -- in case a hole 125 is punctured, the tungsten film of the upper layer which constitutes the W/aluminum/W laminating wiring 120 which is the 2nd-layer wiring 9 **********s, and an interlayer's aluminum film may be exposed
[0065] If the W/aluminum/W laminating wiring 124 which is the 3rd-layer wiring 10 is formed after this aluminum film has been exposed The gas used in case the tungsten film of a lower layer [CVD] is formed following the sputtering method. when the covering nature of the tungsten film deposited by the lower layer sputtering method which constitutes the W/aluminum/W laminating wiring 124 is bad (WF6), The exposed aforementioned aluminum film reacts and it is AlF3. It is generated and defective continuity may arise between the 2nd-layer wiring 9 and the 3rd-layer wiring 10.
[0066] therefore, the thickness of the tungsten film formed by the lower layer sputtering method which constitutes the W/aluminum/W laminating wiring 124 which is the 3rd-layer wiring 10 -- thick -- carrying out -- connection -- the covering nature in the pars basilaris ossis occipitalis of a hole 125 was raised, and the aforementioned defective continuity is prevented
[0067] The tungsten film which constitutes the lower layer of the W/aluminum/W laminating wiring 124 consists of a 0.1 micrometers tungsten film deposited by the sputtering method, and a 0.15-micrometer tungsten film deposited in CVD, and the thickness of 0.6 micrometers and the upper tungsten film of the thickness of an interlayer's aluminum film is 0.05 micrometers.
[0068] drawing 5 -- connection -- the flow yield during the W/aluminum/W laminating wiring located in the upper and lower sides connected through the hole, and connection -- the relation with the aspect ratio of a hole is shown About 40% of flow yield can be obtained for an aspect ratio also as 2.0.
[0069] As mentioned above, although the manufacturing process until it forms the W/aluminum/W laminating wiring 124 which is the 3rd-layer wiring 10 was described, the 4th-layer wiring 11 and the 5th-layer wiring 12 which are formed in the upper layer rather than the 3rd-layer wiring 10 are formed like the W/aluminum/W laminating wiring 124 which is the 3rd-layer wiring 10.
[0070] Moreover, the 3rd layer insulation film 126, 127, and 128 located between the 3rd-layer wiring 10 and the 4th-layer wiring 11 and the 4th layer insulation film 131, 132, and 133 located in a row between the 4th-layer wiring 11 and the 5th-layer wiring 12 are formed like the 2nd layer insulation film 121, 122, and 123. the connection to which the W/aluminum/W laminating wiring 129 which is the 4th-layer wiring 11 was formed in the 3rd layer insulation film 126,127,128 -- it has connected with the W/aluminum/W laminating wiring 124 which is the 3rd-layer wiring 10 through a hole 130
[0071] The W/aluminum/W laminating wiring 134 which is the 5th-layer wiring 12 is covered by the 5th layer insulation film 136, 137, and 138. the connection to which the W/aluminum/W laminating wiring 134 was formed in the 4th layer insulation film 131,132,133 -- it has connected with the W/aluminum laminating wiring 124 through a hole 135 The 5th layer insulation film 136, 137, and 138 is also formed by the same method as the 2nd layer insulation film 121, 122, and 123.
[0072] The thickness of the 5th layer insulation film 137 which deposited the thickness of the 5th layer insulation film 136 by about 0.6 micrometers and the applying method is [the thickness of about 0.6 micrometers and the 5th layer insulation film 138 of the thickness of about 0.55 micrometers and etchback] about 1.2 micrometers.
[0073] On the 5th layer insulation film 136 and 137 and 138, the aluminum wiring (it abbreviates to aluminum wiring below) 139 which is the power supply wiring formed by the manufacturing process of the 6th-layer wiring 13 is formed. the connection to which the aluminum wiring 139 was formed in the 5th layer insulation film 136 and 138 -- it has connected with the W/aluminum/W laminating wiring 134 which is the 5th-layer wiring 12 through a hole 140 this connection -- the size of a hole 140 is 1.5x3.0 micrometers, and an aspect ratio is 1.0
[0074] connection -- a hole 140 is formed by the dry etching method which used RIE (Reactive Ion Etching) or the wet etching method, and the RIE dry etching method Just before forming the aluminum wiring 139, sputter-etching processing is performed into inert gas atmosphere. The thickness of the aluminum wiring 139 is 1.0-2.0 micrometers. In addition, you may use Cu wiring for the 6th-layer wiring 13.
[0075] On the 6th-layer aluminum wiring 139 which is wiring 13, the final passivation films 141 and 142 are formed. The final passivation film 141 is formed for example, by the loculus-ized silicon film, and the final passivation film 142 is formed by the oxidization silicon film.
[0076] On the final passivation film 141 and 142, the BLM (Ball Limiting Metallurgy) film 143 as drawer wiring for external terminals is formed by the sputtering method. The BLM film 143 has structure which carried out the laminating of chromium (Cr), Cu, and the gold (Au) one by one, and the external terminal (bonding pad) 144 is formed on the BLM film 143.
[0077] the connection between the BLM film 143 and the aluminum wiring 139 which is the 6th-layer wiring 13 -- connection -- it is carried out through a hole 145 connection -- or it gives and processes an angle into the final passivation films 141 and 142 by the dry etching method, even the upper surface of the final passivation film 141 is removed by wet etching, after that, the final passivation film 141 is processed by dry etching, and a hole 145 is formed
[0078] such a method -- connection -- forming a hole 145 -- connection -- poor covering of the BLM film 143 in a hole 145 can

be prevented

[0079] As mentioned above, although invention made by this invention person was concretely explained based on the example, it cannot be overemphasized by this invention that it can change variously in the range which is not limited to the aforementioned example and does not deviate from the summary.

[0080] for example, what semiconductor integrated circuit equipment which has multilayer interconnections other than six layer although the aforementioned example explained the case where it applied to the memory LSI with logic of six-layer wiring -- being also alike -- it is applicable

[0081] Moreover, in this invention, it is applicable also to the electronic instrument of mother chip structure which carries two or more semiconductor chips on the wiring substrate which has a multilayer interconnection. The wiring substrate of the aforementioned electronic instrument has the signal wiring of at least three or more layers, and is arranged by the channel structure like the signal wiring of six-layer wiring of the memory LSI with logic. The aforementioned wiring substrate is formed by the single crystal silicon substrate, the silicon-carbide substrate, the ceramic substrate, the mullite substrate, etc.

[0082]

[Effect of the Invention] It will be as follows if the effect acquired by the typical thing among invention indicated by this application is explained briefly.

[0083] (1) it is possible to arrange wiring in a wiring pitch 2.0 micrometers or less in the semiconductor integrated circuit equipment which has a multilayer interconnection according to this invention -- becoming -- moreover, connection -- since the flexibility of the layout of a hole can be increased, multilayering of the high density assembly of wiring and wiring is simultaneously realizable

[0084] (2) the connection which has the aspect ratio of 2.0 in the semiconductor integrated circuit equipment which has a multilayer interconnection according to this invention -- since the wiring of low resistance with sufficient covering nature can be embedded certainly at a hole and wiring can be processed into it using a monolayer resist in a phot lithography processes, improvement in the manufacture yield, improvement in the speed of a working speed, and improvement in the throughput of a wiring process are simultaneously realizable

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[Translation done.]